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NXP, B.V.
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EXAMINER

PERILLA, JASON M

ART UNIT	PAPER NUMBER
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2611

NOTIFICATION DATE	DELIVERY MODE
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10/27/2008

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

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Response to Arguments

1. The Applicant's arguments, filed October 7, 2008, have been fully considered, but they are not persuasive.

The Applicant suggests that the prior art reference Buckland (U.S. Pat. No. 4744081) fails to disclose control circuitry "delaying the clocking of the parallel output portion by preventing one of the first clock pulses from reaching the second clock circuitry."

As applied in the Examiner's final rejection dated August 22, 2008, the claimed first clock pulse is disclosed by Buckland's "SERIAL CLOCK" (fig. 1, ref. 26). The parallel output portion is Buckland's "LATCH" (fig. 1, ref. 18). The parallel output portion is clocked by the "CLOCK" (fig. 1) output from Buckland's clock divider (fig. 1, ref. 20). The clock divider is applied as the claimed second clock circuitry. The second clock circuitry or clock divider is driven by the first clock pulse. Finally, the second clock circuitry takes as input a "SLIP" signal (fig. 1) from Buckland's control circuit (fig. 1, ref. 10) that "prevents" the second clock circuitry from acting upon any received pulses of the first clock.

The Applicant notes that Buckland illustrates a direct connection of the first clock pulse (i.e. "SERIAL CLOCK") to the second clock circuitry (fig. 1, ref. 20) and argues that, because of the direct connection, Buckland can not cover the claimed "preventing one of the first clock pulses from reaching the second clock circuitry." However, Buckland discloses in column 2, lines 60-65:

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The serial clock signal is also supplied to the divider 20 which, in the absence of a signal SLIP supplied from the control circuit 10, frequency divides the clock signal by a factor M to produce a clock signal on a line 28, under the control of which m-bit words from the shift register 16 are latched in the latch 18 (emphasis added).

It is certain that Buckland's second clock circuitry 20 "frequency divides" the first clock pulses. However, Buckland clearly discloses that the second clock circuitry 20 only performs such dividing in the absence of a signal SLIP supplied from the control circuit 10. That is, the first clock pulses are "prevented" from being divided or are "prevented" from reaching the divider of the second clock circuitry in the condition that the SLIP signal is present because such pulses are *only* divided *if* the SLIP signal is not present.

The Applicant, in essence, argues that the lack of a specific "gating control circuit" between the first clock pulses and the second clock circuitry in Buckland's figure 1 is determinative on the point. However, although Buckland does not illustrate such a specific "gating control circuit", Buckland does disclose control circuitry (fig. 1, ref. 10) which outputs a SLIP signal which is applied in the second clock circuitry (fig. 1, ref. 20) as a "gate" to the operation of the circuitry's dividing operation.

With respect to the Applicant's argument that no motivation is shown to combine the prior art references Buckland and Giorgetta et al (U.S. Pat. No. 7035292; "Giorgetta"), the argument is not persuasive. Buckland's frame finding circuitry could be advantageously utilized in an optical receiver and the combination of the two references would produce only routine and predictable results.

Conclusion

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2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M Perilla/
Art Unit 2611
October 15, 2008

/jmp/

/Chieh M Fan/
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